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JAPANESE PATENT OFFICE

## PATENT ABSTRACTS OF JAPAN

(11) Publication number: **63103511 A**(43) Date of publication of application: **09.05.88**(51) Int. Cl. **H03K 3/037**(21) Application number: **61248406**(22) Date of filing: **21.10.86**(71) Applicant: **OKI ELECTRIC IND. CO. LTD.**(72) Inventor: **YOMO MAKOTO  
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KAWAKAMI YASUSHI**(54) **FLIP-FLOP CIRCUIT**

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(57) Abstract

**PURPOSE:** To operate the titled circuit by an input clock pulse at a high frequency normally by adding two basic flip-flop circuits comprising two inverter circuits connecting input and output mutually to an amplification inverter circuit and a flip-flop circuit comprising a transfer gate using a FET.

**CONSTITUTION:** A critical pulse of the circuit starts from a data input terminal D through a FET 1, an amplification inverter 5 via a node N11, through a FET 7 via a node N13, through an amplification inverter 11 via a node N15 and reaches an output terminal Q, and the highest operating frequency of the circuit depends on the propagation delay time characteristic of the FET 1, the amplification inverter 5, the FET 7 and the amplification inverter 11. The fanout number of the FET and the inverter for the critical pulse is less than that of the NOR gate of a conventional circuit and the propagation delay time is decreased. Thus, the highest operating frequency is increased.

